DARE22G

Product Brief

22nm Radiation Hardened Mixed-Signal ASIC Design Platform

DARE22G is a radiation-hardened ASIC design platform for space applications in GF 22nm FDSOI technology. It provides an extensive set of digital and analog IPs along with a design kit to support full-custom design of mixed-signal blocks. DARE22G standard cell libraries and IPs make use of several Radh-Hard-By-Design techniques to mitigate total ionizing dose and single-event effects in harsh environments.

Key Features

- TID tolerance up to 100 krad (SiO_2)
- SEL hardening beyond 70 MeV·cm^2/mg
- SEU hardened flip-flops
- SET hardened clock/asynchronous tree cells
- TMR support
- Multi-Vt and multi-Lg core cell variants enabling fine-grained power vs. delay trade-offs
- Multi-domain I/O support
- Multi-voltage programmable I/O interface
- Cold-spare LVCMOS IO, LVDS and SSTL
- Distributed power-on-control
- Wire-bonding and flip-chip enabled
- Inline and staggered pad arrangement
- Analog IP hardened against SET above 60 MeV·cm^2/mg

Deliverables

Logic synthesis is supported with front-end library views. Black-box views and ADK are provided to assist custom analog design.

- Analog Design Kit (Cadence IC6)
- Black-box CDL netlists
- OA symbol and abstract views
- Encrypted Spectre® netlists
- IBIS models (on demand)
- Synopsys Liberty files
- Compiled Synopsys libraries
- Verilog simulation models
- VITAL simulation models
- HTML datasheets
- User guides

Radiation Hardened IP

DARE22G offers an extensive range of libraries and IP blocks for the implementation of complex mixed-signal ASICs for radiation environment applications.

- High-density 10-track standard cell libraries
  - Multiple Vt (sLVT, LVT, RVT, HVT)
  - Multiple channel lengths (20/24/28 nm)
  - Conventional and Flipped Well
  - Up to 60 MeV·cm^2/mg SEU/SET hardening
  - Special cells supporting TMR
- Multi-voltage I/O library
  - 1.8 V or 3.3 V signal interface
  - 2 – 24 mA programmable drive strength
  - Programmable input pull-up/pull-down
  - Fast speed and slew-rate controlled buffers
- DDR3-compliant SSTL_15 library
  - 1600 Mbps data rate
- Wide-range programmable PLL
  - 8.929 – 2000 MHz output clock
  - 20 – 100 MHz reference clock
  - Single 0.8 V power supply
- LVDS transmitter/receiver
  - > 1 Gbps data rate
  - TIA/EIA-644-A-2001 compliant
  - Fail-safe input signal detection
- Bandgap-based 1.8 V IVREF
  - 0.6 V output reference voltage
  - 10 µA output reference current
  - Digitally trimmable

Analog Design Kit

The DARE22G ADK extends the foundry PDK with additional features to assist full-custom designers in implementing radiation-hardened blocks compatible with DARE22G specifications:

- Schematic checks for Cadence IC6 Virtuoso®
- SET fault injection simulation toolkit for Cadence IC6 environment
- Radiation-hardened layout DRC rule deck for Siemens Calibre®

Technology	
Foundry	GF
Process	22FDX
Supported MiM	No (APMOM/MOM supported)
Supported metal stacks	10M_2Mx_6Cx_2Ix_LB 9M_2Mx_3Cx_2Bx_1Ix_1Ox_LB

Operating Conditions	
Core voltage	0.8 V
LVDS voltage	1.8 V
SSTL voltage	1.5 V (DDR3)
I/O voltage	1.8 V 3.3 V
Junction temperature	-40 – 125 °C
ESD protection	up to 2 kV (HBM)
TID tolerance	100 krad (SiO_2)
SEL tolerance	> 70 MeV·cm^2/mg
SEU tolerance	> 60 MeV·cm^2/mg

Design Services

Imec.IC-link offers design services to implement your radiation-hardened ASICs integrating existing DARE22G and customer-designed IPs. Special digital implementation methodologies are employed to deliver optimal TID and SEE performance.

Imec offers a broad range of chip services to support customers with manufacturing, assembling, testing and validating of flight models based on the DARE22G technology.

Support

Further technical information or design service requests can be obtained at dare@imec.be.