DARE65T

Product Brief

65 nm Radiation Hardened Mixed-Signal ASIC Design Platform

DARE65T is a radiation-hardened ASIC design platform for space applications in TSMC 65 nm Low-Power technology. It provides an extensive set of digital and analog IPs along with a design kit to support full-custom design of mixed-signal blocks. DARE65T standard cell libraries and IPs make use of Rad-Hard-By-Design techniques to mitigate total ionizing dose and single-event effects in harsh environments.

Key Features

- TID tolerance over 300 krad (SiO_2)
- SEL hardening beyond 70 MeV·cm^2/mg
- SEU hardened flip-flops up to 66.3 MeV·cm^2/mg
- SET hardened clock/asynchronous tree cells up to
  - Low hardening: up to 24.5 MeV·cm^2/mg
  - Medium hardening: up to 33.5 MeV·cm^2/mg
  - High hardening: up to 48.5 MeV·cm^2/mg
- TMR support
- Multi-Vt and multi-Lg core cell variants enabling fine-grained power vs. delay trade-offs
- Multi-domain I/O support
- Multi-voltage programmable I/O interface
- Cold-spare LVCMOS IO, LVDS and SSTL
- Distributed power-on-control
- Wire-bonding and flip-chip enabled
- Inline and staggered pad arrangement
- Asynchronous Write-through SRAM with at-speed BIST support
- MBU insensitive SRAM
- Analog IP hardened against SET above 60 MeV·cm^2/mg

Radiation Hardened IP

DARE65T offers an extensive range of libraries and IP blocks for the implementation of complex mixed-signal ASICs for radiation environment applications.

- High-density 12-track standard cell libraries
  - Multiple Vt (LVT, SVT, HVT)
  - Multiple channel lengths (60 nm, 70 nm)
  - Up to 60 MeV·cm^2/mg SEU/SET hardening
  - Special cells supporting TMR
- Multi-voltage I/O library
  - 1.8 V, 2.5 V or 3.3 V signal interface
  - 2, 4, 8, 12, 24 mA programmable drive strength
  - Programmable input pull-up/pull-down
  - Fast speed and slew-rate controlled buffers
  - Input cells with Schmitt-trigger or regular CMOS
- DDR3-compliant SSTL cells at 1.5V
  - 800 Mbps data rate
- DDR2-compliant SSTL cells at 1.8V
  - 800 Mbps data rate
- LVDS transmitter/receiver
  - 400 Mbps data rate
  - TIA/EIA-644-A-2001 compliant
  - Fail-safe input signal detection
- High-density single-port memory compiler
  - 250 MHz minimum operating frequency
  - 256 to 32k bits memory size
  - 8 to 64 bits word width
  - Asynchronous write-through mode for DFT
  - Optional 1-8 bit write-mask
  - At-speed BIST ready
  - Optional guard ring generation
- High-density dual-port memory blocks
  - 250 MHz minimum operating frequency
  - Available w×b configurations: 512×40, 1k×40, 4k×40, 8k×40 and 2k×24
  - Asynchronous write-through mode for DFT
  - At-speed BIST ready
- Wide-range programmable PLL
  - 6.25 to 1200 MHz output clock
  - 20 to 100 MHz reference clock
  - Single 1.2 V power supply
- Bandgap-based 1.2 V IVREF
  - 0.6 V reference voltage
  - 10 µA reference current
  - Digitally trimmable (4 bits)
- Bandgap-based 2.5 V IVREF
  - 0.6 V reference voltage
  - 10 µA reference current
  - Digitally trimmable (4 bits)
    - Accuracy before trimming: < 5%
    - Accuracy after trimming: < 1%
- 1-ksps 10-bit on-chip temperature sensor
  - -40 to 125 °C temperature range
  - Digitally trimmable (4 bits)

Deliverables

Logic synthesis is supported with front-end library views. Black-box views and ADK are provided to assist custom analog design.

- Analog Design Kit (Cadence IC6)
- Black-box CDL netlists
- OA symbol and abstract views
- Encrypted Spectre® netlists
- IBIS models (on demand)
- Synopsys Liberty files
- Compiled Synopsys libraries
- Verilog simulation models
- VITAL simulation models
- HTML datasheets
- User guides

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Analog Design Kit

The DARE65T ADK extends the foundry PDK with additional features to assist full-custom designers in implementing radiation-hardened blocks compatible with DARE65T specifications:

- Schematic checks for Cadence IC6 Virtuoso®
- SET fault injection simulation toolkit for Cadence IC6 environment
- Radiation-hardened layout DRC rule deck for Siemens Calibre®

Technology	
Foundry	TSMC (FAB12)
Process	CMN65LP
MiM	2 fF/µm^2
Metal stack	1P9M6X1Z1U_ALRDL (9 Cu layers + 1 Al layer)

Operating Conditions	
Core voltage	1.2 V ± 10%
LVCMOS I/O voltage	2.5 V ± 10% 1.8 V ± 10% (underdrive) 3.3 V ± 10% (overdrive)
LVDS voltage	2.5 V ± 10%
SSTL voltage	1.5 V ± 5% (DDR3) 1.8 V ± 5% (DDR2)
Junction temperature	-40 to 125 °C
ESD protection	up to 2 kV (HBM)

Design Services

Imec.IC-link offers design services to implement your radiation-hardened ASICs, integrating existing DARE65T and customer IPs. Special digital implementation methodologies are employed to deliver optimal TID and SEE performance.
Imec offers a broad range of chip services to support customers with manufacturing, assembling, testing and validation of flight models based on the DARE65T technology.

Support

Further technical information or design service requests can be obtained at dare@imec.be.