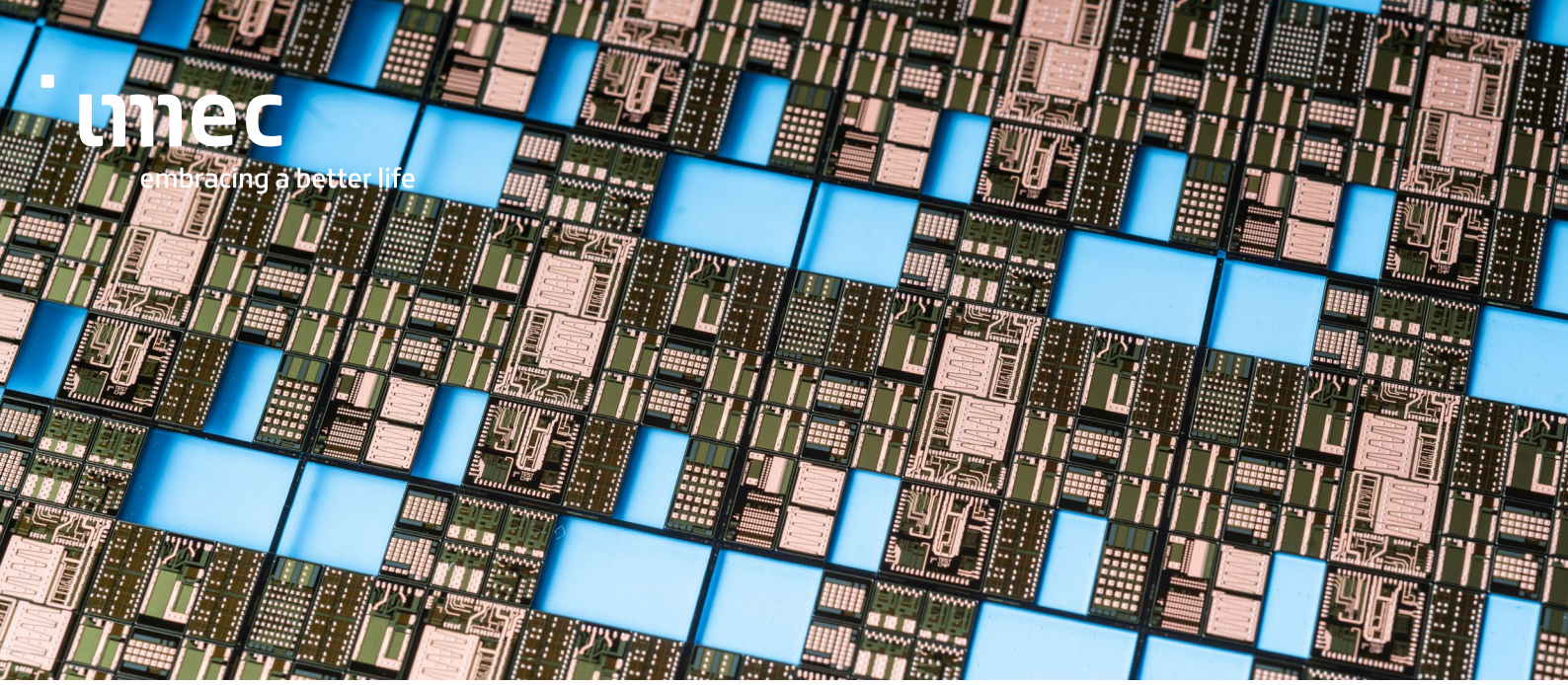

GaN-ICs for monolithic integration of power systems 100V & 650V

To unlock the full potential of GaN power electronics, imec offers a unique GaN-on-SOI process. The deep-trench isolation implemented in this process provides full isolation between power devices, drivers, control and protection circuits. This, in turn, enables the manufacturing of complex GaN ICs. In addition to accommodating smaller form factors, the close proximity of devices drastically reduces parasitic inductance, resulting in a significant switching speed enhancement.

Low-cost MPW and dedicated mask runs

To make GaN-on-SOI devices and circuits more affordable and easily available to its customers, imec offers a Multi-Project Wafer (MPW) service. In this MPW model, mask, processing and engineering costs are shared across multiple customer designs, typically delivering prototyping runs of 40 samples dies. For even larger quantities, dedicated mask runs can also be requested which return approximately 12 x 200mm/8 inch wafers. For even larger productions runs, we offer the possibility of engaging with external manufacturing partners.

State-of-the-art e-Mode mode power devices on 200m/8-inch Si wafer

GaN-based power devices, mainly available as discrete components, have pushed operating frequencies and efficiencies of Switch Mode Power Supplies (SMPS) to record levels. However, the technology's full potential can only be unlocked by reducing the parasitic inductances.

Imec's GaN-on-SOI technology allows to monolithically integrate logic and power components onto the same die in all-GaN technology, addressing high-voltage applications such as Power Factor Correction converters (PFC) with the 650V platform and 48V and 12V power supplies for data centers and AI/Automotive chiplets with the new 100V platform special features.

With imec's GaN-IC technology you are able to:

- Integrate multiple transistors on a single IC using trench isolation
- Save package cost by packaging one instead of multiple devices
- Reduce system parasitic inductance

Picture of a 100V GaN-IC HB switch with driver and temperature sensor

GaN-on-SOI Design Kit

To make this technology more easily available, imec provides an extensive GaN-on-SOI Process Design Kit (PDK), both for 100V and 650V technologies. These kits include process documentation, library devices, layout guidelines for custom design, verification, and models. Low-ohmic and high- ohmic resistors are provided, as well as Metal/Oxide/Metal capacitors, Metal/Insulator/Metal capacitors, and low voltage logic devices. These enable customers to design highly integrated GaN power systems on chip. The PDKs are available after signing imec's GaN-IC Design Kit License Agreement (DKLA).

40 V e-MODE p-GaN HEMT

Datasheet Power Device with W_{eff} = 120 mm

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage			40		V
I_D	Pulsed Drain current	1 ms pulse			24	A
V_{GS}	Gate-Source voltage		-10		7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	40			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T= 25° C		300	<1000	nA/mm
		V_{GS} = 0 V, V_{DS} = 650 V T= 150° C		10	<100	µA/mm
I_{GSS}	Gate-Forward leakage	V_{DS} = 0 V, V_{GS} = 7 V T= 25° C		13	<100	µA/mm
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T= 25° C		2.8	5.5	µA/mm
		V_{GS} = 7 V, V_{DS} = 0.1 V T= 150° C		5.3	8.8	Ω mm
V_{TH}	Gate-Threshold voltage	maximum g_m	2.1	2.5	2.9	V
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V V_{DS} = 20 V f = 100 kHz		0.52		pF/mm
C_{OSS}	Output capacitance			0.69		pF/mm
C_{RSS}	Reverse transfer capacitance			62		pF/mm
DISPER-SION	Dynamic Ron (normalized)	T= 25° C till 150° C, 0-100 Volt range pulsed 10 us on 1990 us off			<25	%

100 V e-MODE p-GaN HEMT

Datasheet Power Device with W_{eff} = 120 mm

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage			100		V
I_D	Pulsed Drain current	1 ms pulse			23	A
V_{GS}	Gate-Source voltage		-10		7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	100			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T= 25° C		300	<1000	nA/mm
		V_{GS} = 0 V, V_{DS} = 650 V T= 150° C		10	<100	µA/mm
I_{GSS}	Gate-Forward leakage	V_{DS} = 0 V, V_{GS} = 7 V T= 25° C		13	<100	µA/mm
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T= 25° C		3.5	6	µA/mm
		V_{GS} = 7 V, V_{DS} = 0.1 V T= 150° C		6.8	10	Ω mm
V_{TH}	Gate-Threshold voltage	maximum g_m	2.1	2.5	2.9	V
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V V_{DS} = 20 V f = 100 kHz		0.52		pF/mm
C_{OSS}	Output capacitance			0.61		pF/mm
C_{RSS}	Reverse transfer capacitance			30		pF/mm
DISPER-SION	Dynamic Ron (normalized)	T= 25° C till 150° C, 0-100 Volt range pulsed 10 us on 1990 us off			<25	%

650 V e-MODE p-GaN HEMT - Datasheet Power Device with W_{eff} = 36 mm

Symbol	Description	Test conditions	Min	Typ	Max	Unit
ABSOLUTE MAXIMUM RATINGS						
BV_{DS}	Drain-Source voltage			>650		V
I_D	Pulsed Drain current	1 ms pulse			7.5	A
V_{GS}	Gate-Source voltage				7	V
ON/OFF STATE CHARACTERISTICS						
BV_{DS}	Drain-Source voltage	V_{GS} = 0 V	650			V
I_{DSS}	Drain-Source leakage	V_{GS} = 0 V, V_{DS} = 650 V T= 25° C		100	1000	nA/mm
		V_{GS} = 0 V, V_{DS} = 650 V T= 150° C		50	500	µA/mm
I_{GSS}	Gate-Forward leakage	V_{DS} = 0 V, V_{GS} = 7 V T= 25° C		20	100	µA/mm
R_{DS-ON}	Drain-Source ON resistance	V_{GS} = 7 V, V_{DS} = 0.1 V T= 25° C		14	18	µA/mm
		V_{GS} = 7 V, V_{DS} = 0.1 V T= 150° C		30	35	Ω mm
V_{TH}	Gate-Threshold voltage	maximum g_m	2.1	2.3	2.9	V

Symbol	Description	Test conditions	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS						
C_{ISS}	Input capacitance	V_{GS} = 0 V V_{DS} = 650 V f = 1 MHz		47.2		pF
C_{OSS}	Output capacitance			14.6		pF
C_{RSS}	Reverse transfer capacitance			0.12		pF

Cointegration of low-side and high-side power devices is possible using GaN-on-SOI substrates as the buried oxide of the SOI, the oxide-filled deep trenches and deep Si contact effectively eliminate the back-gating effect that is common on the GaN-on-Si substrates. Imec's monolithic integration allows the cointegration of the driver, resulting in lower parasitic inductances, unlocking the full potential of the fast-switching speed of GaN power devices.

Further functionality can be added through the low-voltage logic and analog switches, the high-ohmic and low-ohmic resistors and the integrated MIM-capacitors.

Contact details

MPW RUNS

ganmpw@imec-int.com

This leaflet is carbon neutral printed.