imec

DARE - radiation hardening by design

DARE22G

Body Bias Generator

Product Brief

Product Overview

DARE22G BBG implements a body bias voltage generator for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

In such technology, body biasing regulates transistor threshold voltages, directly impacting performance and power consumption. On-chip control of body bias voltages enables dynamic adjustment of transistor characteristics to modulate speed and power trade-offs. Body bias voltage generators can also be integrated with variation monitors to create adaptative tuning mechanisms to compensate PVT variations, aging effects, and radiation-induced degradation during operation.

Features

DARE22G BBG main functionalities include:

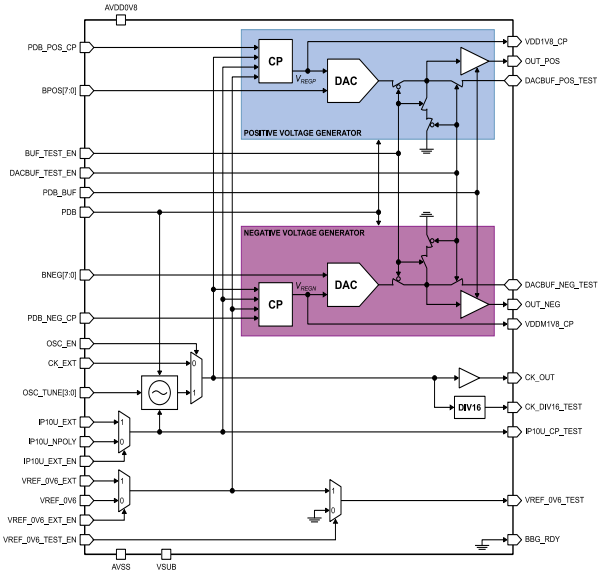
- Dual voltage generation for N-well (0 V to 1.8 V) and P-well (-1.8 V to 0 V) biasing
- 8-bit output voltage selection granularity
- Coverage area up to 9 mm^2 (about 3M gates)
- Power-down mode (< 65 µA)
- Maximum current consumption below 2 mA
- TID immunity over 100 krad (SiO_2)
- SET immunity over 60 MeV.cm^2/mg
- SEL immunity over 70 MeV.cm^2/mg

Block Diagram

The BBG macro mainly consists of an oscillator and two voltage generators based on a common architecture. Each voltage generator employs a charge-pump to produce a regulated reference voltage of either -1.8 V or 1.8 V, which is then scaled by an 8-bit R-2R DAC to provide a biasing signal with the correct output voltage level according to control inputs. Adjusted voltage signals are delivered to the output through analog buffers.

A 100 MHz clock signal is required by the charge-pump circuits and can be either provided externally via the CK_EXT input pin or generated internally by the built-in oscillator. This selection is controlled by the OSC_EN input signal. In active mode (PDB = 1), the internally selected clock signal is buffered out via CK_OUT pin to be used by other system blocks.

Internal cells also require a 10 µA sinking current signal and a 0.6 V reference voltage signal which must be provided via dedicated inputs. Default current and voltage reference inputs are meant to be used for signals directly provided by an instance of the DARE22G IVREF18 IP when it is co-integrated in the chip. Additional external reference inputs and selection control signals are provided for reference signals provided off-chip.



Pin Interface

Pin Name	Type	Description
AVDD0V8	Power	Power supply
AVSS	Ground	Ground supply
VSUB	Ground	P-substrate bias voltage
IP10U_EXT	Analog	External reference current
IP10U_NPOLY	Analog	Reference current from IVREF18 IP
IP10U_CP_TEST	Analog	Mirrored internal reference current
VREF_0V6_TEST	Analog	Internal reference voltage
VREF_0V6_EXT	Analog	External voltage reference
VREF_0V6	Analog	Voltage reference from IVREF18 IP
DACBUF_POS_TEST	Analog	Testing pin for positive voltage generator
DACBUF_NEG_TEST	Analog	Testing pin for negative voltage generator
VDD1V8_CP	Analog	Reference voltage from positive charge pump
VDDM1V8_CP	Analog	Reference voltage from negative charge pump
OUT_POS	Analog	Positive bias voltage output
OUT_NEG	Analog	Negative bias voltage output
PDB	Digital	Full power-down
PDB_POS_CP	Digital	Positive charge-pump power-down
PDB_NEG_CP	Digital	Negative charge-pump power-down
PDB_BUF	Digital	Buffers power-down
IP10U_EXT_EN	Digital	External current reference selection

Pin Name	Type	Description
VREF_0V6_EXT_EN	Digital	External voltage reference selection
VREF_0V6_TEST_EN	Digital	Internal reference voltage test enable
OSC_EN	Digital	Internal oscillator enable
CK_EXT	Digital	External input clock
CK_OUT	Digital	Buffered output clock
CK_DIV16_TEST	Digital	Output clock signal for testing
OSC_TUNE [3:0]	Digital	Oscillator tuning bits
DACBUF_TEST_EN	Digital	DAC/buffer test mode enable
BUF_TEST_EN	Digital	DAC/buffer test selection
BPOS[7:0]	Digital	Positive output level setting
BNEG[7:0]	Digital	Negative output level setting
BBG_RDY	Digital	Ready flag

Physical Dimensions

DARE22G BBG is implemented as a core macro.

IP Name	Width	Height
BBG	401 µm	476 µm

Contact

For further information, please contact us at
dare@imec.be

Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Supply voltage	V_{VDD}	0.72	0.8	0.88	V
Input reference current	I_{P10U}	8	10	12.5	µA
Input reference voltage	V_{BG0V6}	570	600	630	V
Input frequency	f_{CK}	92	100	112	MHz
Operating temperature	T_J	-40	25	125	°C
ESD rating (HBM)	V_{HBM}	2			kV
TID immunity	TID	100			krad (SiO_2)
SET hardening	SET_{th}	60			MeV.cm^2/mg
SEL hardening	SEL_{th}	70			MeV.cm^2/mg