

## Product Overview

DARE22G LDO08 implements a 0.8 V low-dropout regulator for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

This IP delivers a stable voltage with high drive-strength capabilities and provides robustness against power supply, temperature variations, and circuit loading effects.

## Features

DARE22G LDO08 main functionalities include:

- 0.8 V output voltage
- Drive capability up to 100 mA
- Excellent stability over supply voltage, temperature, and load variations
- Low operating current ( $< 125 \mu\text{A}$ )
- Low output voltage noise ( $< 0.05 \text{ mV}_{\text{RMS}}$ )
- Power-down mode ( $< 0.8 \mu\text{A}$ )
- Output disable mode
- TID immunity over 100 krad ( $\text{SiO}_2$ )
- SET immunity over 60  $\text{MeV}\cdot\text{cm}^2/\text{mg}$
- SEL immunity over 70  $\text{MeV}\cdot\text{cm}^2/\text{mg}$

## Block Diagram

The LDO08 macro uses a comparator and a resistive divider connected in a negative-feedback loop to regulate an output driver transistor, ensuring a stable 0.8 V output voltage from a 1.8 V supply input.

The feedback loop must be closed at the top level by connecting the feedback input to the output voltage at the point where accurate regulation is needed.

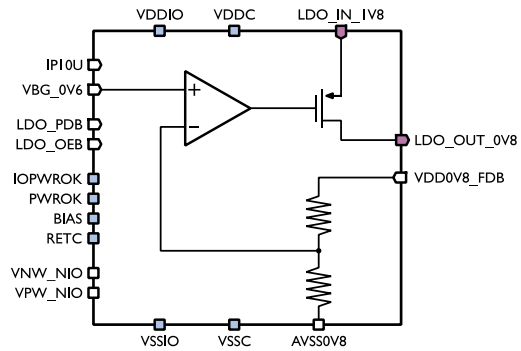
The integrated amplifier requires an external high-precision 10  $\mu\text{A}$  current source and a 0.6 V voltage reference to operate. These signals can be provided on chip by the DARE22G IVREF18 IP. Additionally, an external capacitance of 10  $\mu\text{F}$  is required to stabilize the internal control loop.

Power-down and output enable functionalities support power-saving techniques at system level.

## Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Core supply voltage	$V_{\text{DD}0\text{V}8}$	0.72	0.8	0.88	V
I/O supply voltage	$V_{\text{DD}1\text{V}8}$	1.62	1.8	1.98	V
Operating temperature	$T_j$	-40	25	125	$^{\circ}\text{C}$
ESD rating (HBM)	$V_{\text{HBM}}$	2			kV
TID immunity	TID	100			krad ( $\text{SiO}_2$ )
SET hardening	$\text{SET}_{\text{th}}$	60			$\text{MeV}\cdot\text{cm}^2/\text{mg}$
SEL hardening	$\text{SEL}_{\text{th}}$	70			$\text{MeV}\cdot\text{cm}^2/\text{mg}$



## Pin Interface

Pin Name	Type	Description
VDDIO	Power	I/O power supply rail
VSSIO	Ground	I/O ground supply rail
VDDC	Power	Core power supply rail
VSSC	Ground	Core ground supply rail
IOPWROK	Digital	Pass-through rail (unused)
PWROK	Digital	Pass-through rail (unused)
RETC	Digital	Pass-through rail (unused)
BIAS	Digital	Pass-through rail (unused)
VNW_NIO	Power	1.8 V back-bias voltage
VPW_NIO	Ground	0 V back-bias voltage
IPI0U	Analog	10 $\mu\text{A}$ bias current
VBG_0V6	Analog	0.6 V reference voltage
LDO_IN_1V8	Analog	1.8 V input voltage pad
LDO_OUT_0V8	Analog	0.8 V output voltage pad
VDD0V8_FDB	Analog	Feedback input
LDO_OEB	Analog	Active-low output enable
LDO_PDB	Analog	Active-low power-down

## Physical Dimensions

DARE22G LDO08 is implemented as an I/O macro compatible with 1.8 V domain I/O rings implemented with the DARE22G I/O library.

IP Name	Width	Height
LDO08	700 $\mu\text{m}$	154 $\mu\text{m}$

\* I/O ring area included

## Contact

For further information, please contact us at [dare@imec.be](mailto:dare@imec.be)