DARE - radiation hardening by design

Product Overview

DARE22G PLL implements a complete radiationhardened phase-locked loop IP in the commercial GF 22 nm FDSOI CMOS technology.

Radiation and single-event effects are mitigated by using various radiation-hardened-by-design (RHBD) techniques. Strong drive-strength gates, SET filters and TMR are used in digital circuitry whereas redundancy techniques and RC filters are employed in analog blocks.

Features

DARE22G PLL main functionalities include:

- Wide output frequency range from 1.953 MHz up to 3 GHz
- Wide input frequency range from 20 MHz up to 800 MHz
- Programmable input and output clock dividers
- Built-in clock generation bypassing
- Built-in digital lock detection
- Low RMS period jitter below I ps
- Power-down mode (< 7 μA)
- Maximum current consumption below 30 mA
- SET immunity over 60 MeV.cm²/mg
- SEL immunity over 70 MeV.cm²/mg
- TID tolerance over 100 krad (SiO₂)

Block Diagram

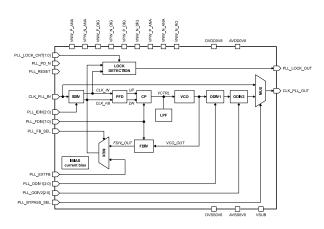
The core of the PLL is composed of a TMR-hardened VCO, a programmable charge pump synchronized with a feedback frequency divider, a PFD, and a second-order LPF. A current bias circuit provides a reference current to the charge pump.

The input clock signal is scaled by the input divider (IDIV) to match the feedback clock signal frequency which is derived from the VCO clock signal after the feedback divider (FDIV) in the PLL core. These two signals are inputs to both the PFD and the lock detection circuit.

The digital lock detection mechanism provides an output flag signal that raises to 1 when input and output clock signals are phase-synchronized.

Two additional dividers (ODIVI & ODIV2) connected in series are used to derive the output clock signal from the VCO output at the desired frequency.

A multiplexer before the clock output pin allows the selection between the generated clock and the input clock signals via an input control signal. Bypassing the generated clock may be useful during initialization or reconfiguration to wait until lock state is achieved.



Pin Interface

PLL_FDIV[7:0] Digital Selection bits for FDIV's division factor PLL_IDIV[2:0] Digital Selection bits for IDIV's division factor PLL_LOCK_CNT Digital Lock detection counter selection bits [1:0] Selection bits Digital PLL_LOCK_OUT Digital Lock detection flag PLL_ODIV1[2:0] Digital Selection bits for ODIV1's division factor PLL_ODIV2[2:0] Digital Selection bits for	AVSSOV8 DVDDOV8 DVSSOV8 CLK_PLL_IN CLK_PLL_OUT PLL_BYPASS_SEL PLL_EXTFB PLL_FB_SEL PLL_FDIV[7:0] PLL_IDIV[2:0]	Power Ground Power Digital Digital Digital Digital Digital Digital	Analog ground supply Digital power supply Digital ground supply Reference input clock Output clock Bypass-mode enable External feedback clock Feedback clock selection Selection bits for FDIV's division factor Selection bits for IDIV's
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ODIVI's division factor PLL_ODIV2[2:0] Digital Selection bits for	LL_ODIV1[2:0]	Digital	Selection bits for
		-	ODIVI's division factor
	LL_ODIV2[2:0]	Digital	Selection bits for ODIV2's division factor
PLL_PD_N Digital Power-down enable	'LL_PD_N	Digital	Power-down enable
PLL_RESET Digital Reset for digital blocks	LL_RESET	Digital	Reset for digital blocks
VNW_N_ANA Ground N-well forward-body voltage for analog blocks	′NW_N_ANA	Ground	
VNW_N_DIG Ground N-well forward-body voltage for digital blocks	'NW_N_DIG	Ground	
VNW_N_RO Power N-well forward-body voltage for VCO	′NW_N_RO	Power	N-well forward-body
VNW_P_ANA Ground N-well reverse-body voltage for analog blocks	'NW_P_ANA	Ground	N-well reverse-body
VNW_P_DIG Power N-well reverse-body voltage for digital blocks	'NW_P_DIG	Power	N-well reverse-body
VPW_N_ANA Ground P-well reverse-body voltage for analog blocks	′PW_N_ANA	Ground	P-well reverse-body
VPW_N_DIG Ground P-well reverse-body voltage for digital blocks	′PW_N_DIG	Ground	P-well reverse-body
VPW_P_ANA Ground P-well forward-body voltage for analog blocks	PW_P_ANA	Ground	P-well forward-body
VPW_P_DIG Power P-well forward-body voltage for digital blocks	′PW_P_DIG	Power	P-well forward-body
VSUB Ground P-substrate bias voltage	'SUB	Ground	

DARE22G Phase-Locked Loop

Product Brief



Physical Dimensions

DARE22G PLL is implemented as a core macro.

IP Name	Width	Height	
PLL	I I 40 μm	603 µm	

Operating Conditions

Contact

For further information, please contact us at <u>dare@imec.be</u>

Performance and reliability are not guaranteed outside these recommended operating boundaries.

Parameter	Name	Minimum	Typical	Maximum	Unit
Analog supply voltage	V_{AVDD}	0.72†	0.8	0.88	V
Digital supply voltage	V_{DVDD}	0.72†	0.8	0.88	V
Operating temperature	T	-40	25	125	°C
TID immunity	TID	100			krad (SiO ₂)
SET hardening	SET _{th}	60			MeV.cm ² /mg
SEL hardening	SEL _{th}	70			MeV.cm ² /mg

[†] Minimum analog & digital supply voltage is specified at 0.76 V for maximum VCO frequency of 3 GHz