imec

DARE - radiation hardening by design

# DARE22G

## 0.8 V Power-On-Reset

Product Brief

## Product Overview

DARE22G POR08 implements a 0.8 V supply power-on-reset circuit for radiation-hardened applications in the commercial GF 22 nm FDSOI CMOS technology.

This IP supports a range of DARE22G digital and mixed-signal IP blocks that require power-on reset signals in the 0.8 V supply domain.

## Features

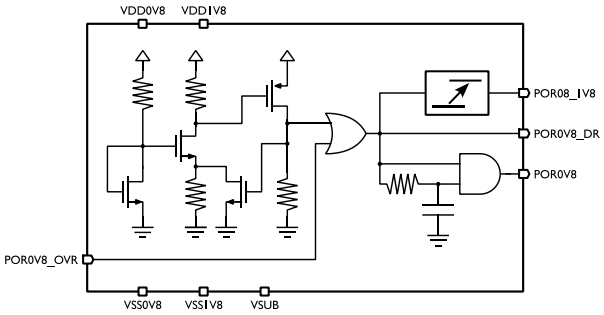
DARE22G POR08 main functionalities include:

- 0.8 V output reset signal
- 1.8 V level-shifted output reset signal
- 0.8 V glitch-filtered output reset signal
- External reset assertion override
- Positive-going trip point range of 362 - 734 mV
- Negative-going trip point range of 362 - 613 mV
- Hysteresis range of 0 - 91 mV
- Low operating current (< 75 µA)
- TID immunity over 100 krad ($SiO_2$)
- SET immunity over 60 MeV.cm$^2$/mg
- SEL immunity over 70 MeV.cm$^2$/mg

## Block Diagram

The POR08 macro generates a reset signal when the 0.8 V power supply is first applied to the chip and keeps it asserted until the supply voltage reaches its nominal value. It employs a dual-threshold open-drain architecture, with trip points determined by the combined threshold voltages of LVT PMOS and NMOS transistors.

The internally generated reset signal in the 0.8 V domain is output directly via the POR0V8_DR pin, with a glitch-filtered replica provided through the POR0V8 pin. Additionally, a built-in level-shifter translates the internal reset signal to a 1.8 V domain version, which is distributed via the POR08_1V8 pin.




The power-on reset functionality can be combined with an external 0.8 V reset signal provided via the POR0V8_OVR pin. When asserted, this input signal will override the internally generated reset signal.

## Pin Interface

| Pin Name | Type | Description |
|---|---|---|
| VDD1V8 | Power | I/O power supply |
| VSS1V8 | Ground | I/O ground supply |
| VDD0V8 | Power | Core power supply |
| VSS0V8 | Ground | Core ground supply |
| VSUB | Ground | P-substrate bias voltage |
| POR0V8 | Digital | 0.8 V glitch-filtered reset output |
| POR0V8_DR | Digital | 0..8 V reset output |
| POR08_1V8 | Digital | 1.8 V reset output |
| POR0V8_OVR | Digital | Reset override input |

## Physical Dimensions

DARE22G POR08 is implemented as a core macro.

| IP Name | Width | Height |
|---|---|---|
| POR08 | 108 µm | 66 µm |

## Contact

For further information, please contact us at dare@imec.be

## Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

| Parameter | Name | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Core supply voltage | $V_{DD0V8}$ | 0.72 | 0.8 | 0.88 | V |
| I/O supply voltage | $V_{DD1V8}$ | 1.62 | 1.8 | 1.98 | V |
| Operating temperature | $T_J$ | -40 | 25 | 125 | °C |
| TID immunity | TID | 100 | | | krad ($SiO_2$) |
| SET hardening | $SET_{th}$ | 60 | | | MeV.cm$^2$/mg |
| SEL hardening | $SEL_{th}$ | 70 | | | MeV.cm$^2$/mg |