# Product Overview

DARE22G SSTL12 provides single-ended and differential transceiver I/O cells for the implementation of radiation-hardened DDR4 interfaces in the commercial GF 22 nm FDSOI CMOS technology.

DARE22G SSTL12 library also includes a voltage reference generator and I/O supply cells for the implementation of SSTL domains compatible with I/O rings based on the DARE22G I/O library.

DARE22G exploits the intrinsic SEL immunity provided by the FDSOI technology in combination with special radiation-hardening-by-design (RHBD) techniques to mitigate TID and single-event effects in I/O rings.

DARE22G SSTL12 interfaces are fully compliant with the DDR4 standard and can achieve data signaling rates up to 3.2 Gbit/s. DARE22G supports different configurations for transmitter drivers ($R_{ON}$) and receiver on-die terminations (ODT).

# Features

DARE22G SSTL12 library features include:

- 1.2 V I/O supply domain cells
- Pad-limited fixed-height narrow layout
- Distributed power-on control
- Cold spare functionality
- 2 kV ESD protection (HBM)
- SET immunity over 60 MeV.cm$^2$/mg
- SEL immunity over 70 MeV.cm$^2$/mg
- TID immunity over 100 krad ($SiO_2$)

# SSTL Transceivers

DARE22G SSTL12 transceivers cells are available in both single-ended (RXTX_SE) and differential (RXTX_DIFF) variations. These I/O cells are configurable to operate in either transmitter or receiver mode.

## Cell Features

SSTL12_RXTX main functionalities include:

- Data transfer rates up to 3.2 Gbit/s
- Power-down mode (< 80 µA)
- Two driving capabilities $R_{ON}$ (34 and 40 Ω)
- Multiple ODT configurations (34 to 240 Ω)
- Digital $R_{ON}$/ODT calibration for process variation compensation
- Configurable reference voltage (0.65 to 1.19 V)
- Pseudo-Open Drain for low power consumption

## Pin Interface

| Pin Name | Type | Description |
|---|---|---|
| VDDIO | Power | I/O power supply |
| VSSIO | Ground | I/O ground supply |
| VDDC | Power | Core power supply |
| VSSC | Ground | Core ground supply |
| VREF | Analog | Internal reference voltage |
| PWROK | Analog | Core supply voltage flag |
| PDB | Digital | Power-down enable |
| DS[2:0] | Digital | Impedance selection |
| ZQ_TUNE [2:0] | Digital | ODT calibration bits |
| DIN | Digital | TX core input |
| PADN<br>PADP | SSTL | TX outputs or RX inputs (differential cell) |
| PAD | SSTL | TX output or RX input (single-ended cell) |
| DOUT | Digital | RX core output |

## Physical Dimensions

DARE22G SSTL12 is implemented in the same pad-limited fixed-height narrow layout template defined by the DARE22G I/O library.

| Cell Name | Width | Height |
|---|---|---|
| SSTL12_RXTX_SE | 150 µm | 89 µm |
| SSTL12_RXTX_DIFF | 300 µm | 89 µm |

# Contact

For further information, please contact us at dare@imec.be

# Operating Conditions

Performance and reliability are not guaranteed outside these recommended operating boundaries.

| Parameter | Name | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| Core supply voltage | $V_{DD0V8}$ | 0.72 | 0.8 | 0.88 | V |
| I/O supply voltage | $V_{DD1V2}$ | 1.14 | 1.2 | 1.26 | V |
| Operating temperature | $T_J$ | -40 | 25 | 125 | °C |
| ESD rating (HBM) | $V_{HBM}$ | 2 | | | kV |
| TID immunity | TID | 100 | | | krad ($SiO_2$) |
| SET hardening | $SET_{th}$ | 60 | | | MeV.cm$^2$/mg |
| SEL hardening | $SEL_{th}$ | 70 | | | MeV.cm$^2$/mg |